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April 27, 2000

BOX PATENT APPLICATION
Assistant Commissioner for Patents
Washington, D.C. 20231

Re: Application of Shigeru SEMBONMATSU and Manabu ISHIKAWA
TRAY FOR SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE
Our Ref. Q059017

Dear Sir:

Attached hereto is the application identified above including 23 sheets of the specification and claims, 9 sheets of formal drawings, the executed Assignment and PTO 1595 form, and the executed Declaration and Power of Attorney. Also enclosed is an Information Disclosure Statement with form PTO-1449 and references.

The Government filing fee is calculated as follows:

Total claims	9	- 20	=		x	$18.00	=	
Independent claims	1	- 3	=		x	$78.00	=	
Base Fee								$690.00
TOTAL FILING FEE								**$690.00**
Recordation of Assignment								$40.00
TOTAL FEE								**$730.00**

Checks for the statutory filing fee of $690.00 and Assignment recordation fee of $40.00 are attached. You are also directed and authorized to charge or credit any difference or overpayment to Deposit Account No. 19-4880. The Commissioner is hereby authorized to charge any fees under 37 C.F.R. §§ 1.16 and 1.17 and any petitions for extension of time under 37 C.F.R. § 1.136 which may be required during the entire pendency of the application to Deposit Account No. 19-4880. A duplicate copy of this transmittal letter is attached.

Priority is claimed from April 30, 1999 based on Japanese Application No. 124326/99. The priority document are enclosed herewith.

Respectfully submitted,
SUGHRUE, MION, ZINN,
MACPEAK & SEAS, PLLC
Attorneys for Applicant

By: _____
J. Frank Osha
Registration No. 24,625

TITLE OF THE INVENTION

Tray for Semiconductor Integrated Circuit Device

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention generally relates to a tray for storing a semiconductor integrated circuit device and, more particularly, to a tray for storing a semiconductor integrated circuit device such as a ball grid array type or pin grid array type semiconductor device which has wiring terminals on the lower surface of its package.

Related Background Art

As the package types of semiconductor devices, ball grid array type and pin grid array type are well known. In the former type, as shown in Figs. 1 and 2, ball terminals 1 serving as wiring terminals are arranged in a matrix on the lower surface of a package 2. The package 2 shown in Figs. 1 and 2 is comprised of a substrate 3 and a molded resin 4 covering the upper portion of the substrate 3. In the latter type, lead pins (not shown) are used in place of ball terminals 1. Both of these types have features that the number of wiring terminals can be increased and that electric noise is small, compared to a general quad flat package.

Generally, a ball grid array type ("BGA")

semiconductor device 5, or a pin grid array type ("PGA") semiconductor device is stored in the storage portion of an exclusive tray to be transported or subjected to tests. A storage portion in a conventional tray is a recess having almost the same shape as that of the package of the semiconductor device. The terminals of the semiconductor device should not be brought into contact with the tray. Therefore, through holes or recesses for receiving a ball terminal group or lead pin group are formed in the central portion of the bottom surface of the storage portion. Accordingly, the conventional tray supports the peripheral portion (a portion outside the outermost ball terminals or lead pins and indicated by reference numeral 2 in, e.g., Fig. 2) of the lower surface of the package of the semiconductor device with the peripheral portion of the bottom surface of its storage portion, and restrains horizontal movement of the package with the wall surface of the storage portion.

When the width of the peripheral portion of the lower surface of the package is small, the ball terminals or lead pins may come into contact with the inner wall surface of the terminal-accepting hole, or the edge of the package may enter the hole. Particularly, this problem becomes conspicuous in recent years because, as the package becomes more and

more compact, the width of the peripheral portion of the lower surface of the package becomes narrow.

SUMMARY OF THE INVENTION

It is an object of the present invention to provide a tray for storing a semiconductor device, such as a BGA device or PGA device, having wiring terminals on the lower surface of its package, which can reliably support the semiconductor device regardless of the width of the peripheral portion of the lower surface of the package without causing the wiring terminals to come into contact with the wall surface of the storage portion.

In order to achieve the above object, according to the present invention, there is provided a tray for a semiconductor device such as a BGA device, comprising a substantially planar main body and a first storage portion provided on a first surface of the main body for storing the semiconductor device. The first storage portion has a first wall surface adapted to be arranged around the semiconductor device upon storing the semiconductor device. Also, the first wall surface has a first area which is inclined with an angle so as to support an edge of the package of the semiconductor device but not to come into contact with the wiring terminals.

With this arrangement, the inclined first area

can come into contact with only the edge of the package to support the package.

In order to stabilize the semiconductor device stored in the storage portion, the first wall surface is preferably formed with a second area extending upward from an upper edge of the first area. It is effective if this second area is inclined with an angle larger than the angle of the first area.

The tray according to the present invention is also characterized by further comprising a second storage portion provided on a second surface of the tray main body opposite to the first storage portion, that can store a semiconductor device with wiring terminals thereof facing upward when the tray is turned over, wherein when a tray of the same type is stacked on this tray, the second storage portion of one tray cooperates with the first storage portion of the other tray to form a space for storing the semiconductor device.

With this arrangement, the vertical movement of the semiconductor device stored in the tray can be minimized or suppressed. When the trays are stacked and turned over, the semiconductor device can be easily transported to the second storage portion of the lower tray.

The second storage portion may comprise a second

wall surface having a third area which is arranged around the semiconductor device upon storing the semiconductor device with the wiring terminals thereof facing upward, and which is inclined with an angle so as to support the edge of the package of the semiconductor device. When the tray has such a inclined area, the semiconductor device can be supported with only the edge of its package.

When the package of the semiconductor device has a rectangular or square lower surface, the first storage portion is preferably comprised of four first wall surfaces arranged to form a rectangular or square shape, and the first areas of the first wall surfaces preferably respectively support edges of the lower surface of the package of the semiconductor device.

The present invention will be more fully understood from the detailed description given hereinbelow and the attached drawings, which are given by way of illustration only and are not to be considered as limiting the present invention.

Further scope of applicability of the present invention will become apparent from the detailed description given hereinafter. However, it should be understood that the detailed description and specific examples, while indicating preferred embodiments of the invention, are given by way of illustration only, since

various changes and modifications within the spirit and scope of the invention will be apparent to those skilled in the art from this detailed description.

BRIEF DESCRIPTION OF THE DRAWINGS

In the course of the following detailed description, reference will be made to the attached drawings in which:

Fig. 1 is a side view showing a BGA semiconductor device that can be stored in a tray according to the present invention;

Fig. 2 is a bottom view of the BGA device as shown in Fig. 1;

Fig. 3 is a plan view showing a tray that is constructed in accordance with the present invention for storing the BGA devices;

Fig. 4 is an enlarged plan view showing a portion IV of Fig. 3;

Fig. 5 is a bottom view of the same portion as that shown in Fig. 4;

Fig. 6 is a sectional view taken along the line VI - VI of Fig. 4;

Fig. 7 is a sectional view taken along the line VII - VII of Fig. 4;

Fig. 8 is a sectional view taken along the same sectional position as in Fig. 6, showing a state wherein two trays each shown in Fig. 3 are stacked;

Fig. 9 is a sectional view taken along the same sectional position as in Fig. 6, showing a state wherein a BGA device is arranged in the storage portion on the lower side of the tray shown in Fig. 3;

Fig. 10 is a sectional view taken along the same sectional position as in Fig. 6, showing a modification of a tray according to the present invention; and

Fig. 11 is a sectional view taken along the same sectional position as in Fig. 6, showing another modification of a tray according to the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENT

Referring now to the drawings, and particularly, to Fig. 3, there is shown a tray 10 for storing BGA devices, having an improved construction in accordance with the present invention. The BGA device for use in the tray 10 is one shown in Fig. 1 or 2, being designated by reference numeral 5. The BGA device has a package whose lower surface is substantially square in shape. In this specification, it is to be understood that such terms as "upper", "lower", and the like are used with reference to the ordinary use state of the tray 10, i.e., a state wherein the tray 10 is set horizontally, unless otherwise specified. In the state of Fig. 3, note that the surface which can be seen will be referred to as the upper surface of the

tray 10, and that the surface which cannot be seen will be referred to as the lower surface of the tray 10.

The tray 10 of the present invention can be made from various types of materials in accordance with various types of methods. Especially, the tray 10 molded of a heat-resistant and electro-conductive synthetic resin, e.g., a polyphenylene ether-based resin mixed with a conductive filler such as carbon particles or fiber, or metal particles or fiber, a polyether sulfone-based resin, a polyether imide-based resin, a polyacryl sulfone-based resin, or a polyester-based resin is preferable, because it facilitates the manufacture, is lightweight and is easy to handle. The reason why the conductive synthetic resin is preferable is that charging in the semiconductor device to be stored must be prevented, since the semiconductor device can be damaged by static electricity.

The tray 10 shown in Fig. 3 comprises a substantially rectangular and planar main body 11. The tray 10 has a plurality of linear ridges 12 formed on the upper surface of the tray main body 11, which include those extending parallel to the longitudinal direction (long sides) of the tray 10 and those extending parallel to the widthwise direction (short sides) of the tray 10. Longitudinal ridges 12a are

arranged with constant intervals, and widthwise ridges 12b are arranged at the same constant intervals. In this manner, the ridges 12 are arranged to form a matrix, and each hollow portion of the matrix, i.e., a portion surrounded by a pair of adjacent longitudinal ridges 12a and a pair of adjacent widthwise ridges 12b serve as a first storage portion 14 for storing one BGA device 5.

When a plurality of trays 10 are used as they are stacked on each other, ridges 12e arranged at the outermost peripheral portion of the tray 10 fit with the inner sides of outer frames 16 projecting downward from the peripheral edge of the upper tray 10, to serve as a positioning means for positioning the tray 10 and for preventing lateral misalignment of the tray 10 (see Fig. 8).

Fig. 4 is an enlarged plan view showing a portion IV of Fig. 3, and Fig. 5 is a bottom view of the same portion as that shown in Fig. 4. Fig. 6 is a sectional view taken along the line VI - VI of Fig. 4, and Fig. 7 is a sectional view taken along the line VII - VII of Fig. 4. As is understood from Figs. 4 to 7, each storage portion 14 can store the BGA device 5 having a package 2 with a substantially square lower surface. Hence, first wall surfaces 18 of the four ridges 12 surrounding each storage portion 14 have the same shape

and same size. As shown in Figs. 6 and 7, the storage portion 14 is partitioned into a lower region 20 and an upper region 22 in the vertical direction.

The lower region 20 of the storage portion 14 supports the BGA device 5 when the BGA device 5 is stored horizontally and appropriately, and serves as the main region of the storage portion 14. The lower, first wall surface areas (to be referred to as "lower wall surfaces" hereinafter) 24 of the respective ridges 12 of the lower region 20 are more inclined toward the center of the storage portion 14. In other words, the distance, indicated by L_1 in Fig. 6, between the upper ends of the lower wall surfaces 24 that oppose each other is slightly larger than a length L_0 of one side of the package 2 shown in Figs. 1 and 2, and the distance, indicated by L_2 in Fig. 5, between the lower ends of the lower wall surfaces 24 is smaller than L_0.

Therefore, when the BGA device 5 is moved downward in the horizontal state from above to the lower region 20 of the storage portion 14, the respective lower edges of the lower surface of the package 2 come into contact with the corresponding inclined lower wall surfaces 24 and are supported by them, as indicated by a phantom line in Figs. 4, 6, and 7. As described above, since the four lower wall surfaces 24 surrounding one storage portion 14 have the

same size and the same shape, the BGA device 5 is supported horizontally at the same height of the four lower wall surfaces 24.

In this manner, since the BGA device 5 is supported at only the lower edges of the package 2, it can be supported even if the width, indicated by W in Fig. 2, of the peripheral portion 6 of the lower surface of the package 2 is smaller than the reference size.

Note that when the BGA device 5 is supported, the ball terminals 1 should not come into contact with the lower wall surfaces 24 of the storage portion 14. Hence, the angle of the lower wall surfaces 24 with respect to the horizontal plane, indicated by α in Fig. 6, must be necessarily larger than the angle formed by the lower edges of the package 2 and the outermost ball terminals 1, indicated by β in Fig. 1. Even when this condition is satisfied, if the angle α of the lower wall surfaces 24 becomes less than 40°, the BGA device 5 may be moved in the storage portion 14 when a very small vibration is applied to the tray 10. Therefore, the angle α is preferably 40° or more. Also, when the angle α of the lower wall surfaces 24 exceeds 70°, the package 2 bites into the lower wall surfaces 24 and becomes difficult to remove. Therefore, the angle α is preferably 70° or less.

Further, while the BGA device 5 is supported, the ball terminals 1 should not come into contact with a bottom surface 26 of the storage portion 14. For this reason, the height, indicated by H_1 in Fig. 6, from the bottom surface 26 of the storage portion 14 to a package support point S is set larger than the length, indicated by h in Fig. 1, from the lower surface of the package 2 to the lower ends of the ball terminals 1.

When the BGA device 5 supported by the lower wall surfaces 24 is displaced, second wall surface areas (to be referred to as "upper wall surfaces" hereinafter) 28 of the respective ridges 12 in the upper region 22 of the storage portion 14 restrain this displacement. The angle, indicated by γ in Fig. 6, of the upper wall surfaces 28 with respect to the horizontal plane is set larger than the angle α of the lower wall surfaces 24 and is preferably 85° to 90°. In this manner, with the upper wall surfaces 28 sharply rising from the upper edges of the lower wall surfaces 24, even if the BGA device 5 is displaced in the horizontal direction, when the lower edges of the package 2 reach boundaries 30 between the lower and upper wall surfaces 24 and 28, further horizontal movement of the BGA device 5 is prohibited by the upper wall surfaces 28.

The height, indicated by H_2 in Fig. 6, from the package support point S to the upper edges of the upper

wall surfaces 28 is preferably larger than the thickness of the package 2. Then, for example, when a flat plate (not shown) is placed on the tray 10, the BGA device 5 is completely stored in the space surrounded by the lower surface of the flat plate and the storage portion 14, and can be avoided from being interfered with the flat plate. In order to allow the BGA device 5 to be stored in the storage portion 14 easily, the upper edges of the upper wall surfaces 28 are preferably chamfered as indicated by numerals 32.

The lower and upper wall surfaces 24 and 28 described above need not extend over the entire lengths of the ridges 12 surrounding the storage portion 14. In the shown embodiment, the ridges 12 at the corners of the storage portion 14 may be formed thin. In this case, the corners of the package 2 float.

With BGA device storage trays, for example, when the ball terminals 1 are to be inspected, sometimes the empty second tray is stacked on the first tray storing the BGA devices 5, and these trays are turned over in the stacked state, so that the ball terminals 1 of the BGA devices 5 face upward. Generally, storage portions are formed on the lower side of the second tray as well so that the second tray can also store the BGA devices when the trays are turned over.

Hence, the tray 10 of the shown embodiment also

has a plurality of second storage portions 34 in its lower side. These lower side storage portions 34 correspond in number to the upper side storage portions 14 described above, and are formed immediately under the upper side storage portions 14. Accordingly, as shown in Fig. 8, when a tray 10B of the same type as a tray 10A is stacked on the tray 10A and outermost ridges 12e of the lower tray 10A and an outer frame 16 of the upper tray 10B are engaged with each other, each lower side storage portion 34 of the upper tray 10B is located to cover a corresponding upper side storage portion 14 of the lower tray 10A, so that a space for storing one BGA device 5 is formed between these storage portions 14 and 34.

This will be described in more detail. As is understood from Fig. 5, each storage portion 34 on the lower side of the tray 10 is made up of four projecting pieces 36 projecting downward from the lower surface of the tray main body 11. The projecting pieces 36 are arranged at the corners of the storage portion 34, i.e., positions corresponding to the intersections of the ridges 12 on the upper surface of the tray 10. The projecting pieces 36 each forming an L shape when seen in a horizontal section and are positioned such that their inner wall surfaces or second wall surfaces 38 restrain the corners of the package 2. When the two

trays 10A and 10B are stacked, the four projecting pieces 36 defining one lower side storage portion 34 are fitted with the corner portions of the corresponding upper side storage portion 14, and outer wall surfaces 40 of the respective projecting pieces 36 face the inner surfaces of the thin portions of the ridges 12. In this state, a bottom surface 26 of the upper side storage portion 14 of the lower tray 10A, a bottom surface 42 of the lower side storage portion 34 of the upper tray 10B, the linear ridges 12, and the projecting pieces 36 form a closed space. The BGA device 5 is stored in this space such that its movement is prevented or minimized in the vertical direction as well.

The minimum distance between the opposing wall surfaces 38 is larger than the maximum length of the BGA package 2. Hence, when the tray 10 is turned over and the BGA devices 5 are stored in its lower storage portions 34, the upper surfaces of the packages 2 are in contact with the bottom surfaces 42 of the storage portions 34, as shown in Figs. 5 and 9.

In the above embodiment, the sizes, positions, and shapes of the respective parts of the storage portions 14 and 34, the inclination angles of the wall surfaces 18 and 38, and the like may be changed in various manners in accordance with the size of the BGA

device to be handled, the material of the package, and the like, and may be adjusted through experiments and simulations. For example, the possible movement of the BGA device 5 occurred when a vibration is applied to the tray 10 includes various types. The lower edges of the package may slide on the lower wall surfaces 24 in the longitudinal or widthwise direction of the tray 10. Alternatively, the BGA package 2 may vertically move to come into contact with the lower surface of the upper tray 10B, may rotate about the central point of the BGA 5 as the center, or may swing about opposing corners as fulcrums. Therefore, conditions with which the ball terminals 1 do not always come into contact with the surfaces of the tray 10 must be determined while considering the fact that these movements can occur in the BGA device 5. When satisfying these conditions, the wall surfaces 24, 28, and 38 need not always be flat surfaces, but may be modified to be curved to form projections or recesses.

Although the preferred embodiment of the present invention has been described in detail so far, the present invention is not limited by it. For example, in the above embodiment, the projecting pieces 36 on the lower side of the tray do not support the BGA device 5. However, as shown in Fig. 10, the inner wall surfaces of the projecting pieces 36 may form as

inclined surfaces or third wall surface areas 44, and the upper edges of the package 2 may be supported by the wall surfaces 44. Alternatively, as shown in Fig. 11, step portions 46 may be formed on the inner wall surfaces of the projecting pieces 36, and the peripheral portion of the upper surface of the package 2 may be supported by the step portions 46.

In the above embodiment, the present invention is applied to the BGA device tray 10. The present invention may also be applied to a tray for storing PGA devices or other semiconductor devices each having wiring terminals on the lower surface of the package.

Although, the above embodiment can store a semiconductor device with a substantially square package, the present invention may be applied to a semiconductor device having a package of another shape. In such a case, inclined wall surface areas for supporting the edges of the package may be formed on the wall surfaces of the storage portion that surround the semiconductor device continuously or discontinuously.

As has been described above, with the tray according to the present invention, even if the wiring terminal portions are disposed at positions near the peripheral edge of the lower surface of the package of a semiconductor device, the tray can support the

semiconductor device. Since this support is achieved at only the edges of the package, ball terminals can be prevented from coming into contact with the wall surfaces or bottom surface of the storage portion. Therefore, with the tray of the present invention, when a semiconductor device is stored and transported, damage, deformation, and contamination of the ball terminals caused by contact with the wall surface of the storage portion can be prevented.

From the invention thus described, it will be obvious that the invention may be varied in many ways. Such variations are not to be regarded as a departure from the spirit and scope of the invention, and all such modifications as would be obvious to one skilled in the art are intended for inclusion within the scope of the following claims.

WHAT IS CLAIMED IS:

1. A tray for storing a semiconductor integrated circuit device having a package and wiring terminals on a lower surface of the package, said tray comprising:

a substantially planar main body; and

a first storage portion provided on a first surface of said main body for storing the semiconductor integrated circuit device, said first storage portion having a first wall surface adapted to be arranged around the semiconductor integrated circuit device when the semiconductor integrated circuit device is stored in said first storage portion,

wherein said first wall surface has a first area which is inclined with an angle so as to support an edge of the package of the semiconductor integrated circuit device and to prevent said first wall surface from coming into contact with the wiring terminals of the semiconductor integrated circuit device when the semiconductor integrated circuit device is stored in said first storage portion.

2. A tray according to claim 1, wherein said first wall surface has a second area extending from said first area in a direction apart from said first surface of said main body, and wherein said second area is inclined with an angle larger than the angle of said first area.

3. A tray according to claim 1, wherein said first storage portion is designed so as to prevent said first surface of said main body from coming into contact with the wiring terminals of the semiconductor integrated circuit device when the semiconductor integrated circuit device is stored in said first storage portion.

4. A tray according to claim 1, wherein said main body includes a plurality of intersecting ridges provided on said first surface thereof, and wherein said first storage portion is defined by a first pair of adjacent ones of said ridges and a second pair of adjacent ones of said ridges extending transversely to said first pair.

5. A tray according to claim 4, wherein each of said first and second pairs of ridges defining said first storage portion has a wall surface for serving as said first wall surface, whereby said wall surfaces of said first and second pairs of ridges respectively support edges of the lower surface of the rectangular package of the semiconductor integrated circuit device.

6. A tray according to claim 1, further comprising a second storage portion provided on a second surface of said main body opposite to said first storage portion,

wherein said second storage portion can store a

semiconductor integrated circuit device with wiring terminals thereof facing upward when said tray is turned over, and

wherein when two of said trays are aligned in a stacked relationship, said second storage portion of one tray cooperates with said first storage portion of the other tray to form a space for storing the semiconductor integrated circuit device.

7. A tray according to claim 6, wherein said second storage portion has a second wall surface adapted to be arranged around the semiconductor integrated circuit device when the semiconductor integrated circuit device is stored in said second storage portion with the wiring terminals thereof facing upward, and

wherein said second wall surface has a third area which is inclined with an angle so as to support an edge of the package of the semiconductor integrated circuit device when the semiconductor integrated circuit device is stored in said second storage portion.

8. A tray according to claim 6, further comprising positioning means for positioning said stacked trays to each other.

9. A tray according to claim 6, wherein said main body includes a plurality of projecting pieces provided on said second surface thereof for defining

said second storage portion, and wherein each of said projecting pieces has a wall surface for serving as said second wall surface, whereby said wall surfaces of said projecting pieces respectively support corners of the rectangular package of the semiconductor integrated circuit device.

ABSTRACT OF THE DISCLOSURE

A tray for storing a semiconductor device such as a BGA device. This tray comprises a storage portion for receiving and storing the BGA device therein. The storage portion has a wall surface which is arranged around the semiconductor device upon storing the semiconductor device. This wall surface has an area which is inclined with an angle so as to support an edge of a package of the semiconductor device but not to come into contact with wiring terminals thereof. With this arrangement, the inclined are comes into contact with only the edge of the package so as to be able to support the package.

Fig.1

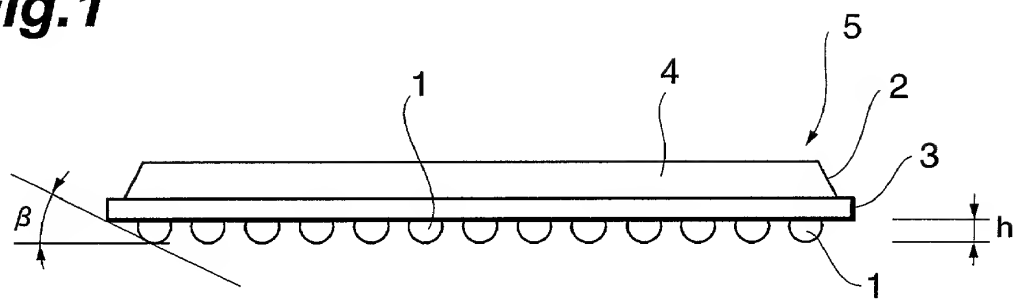
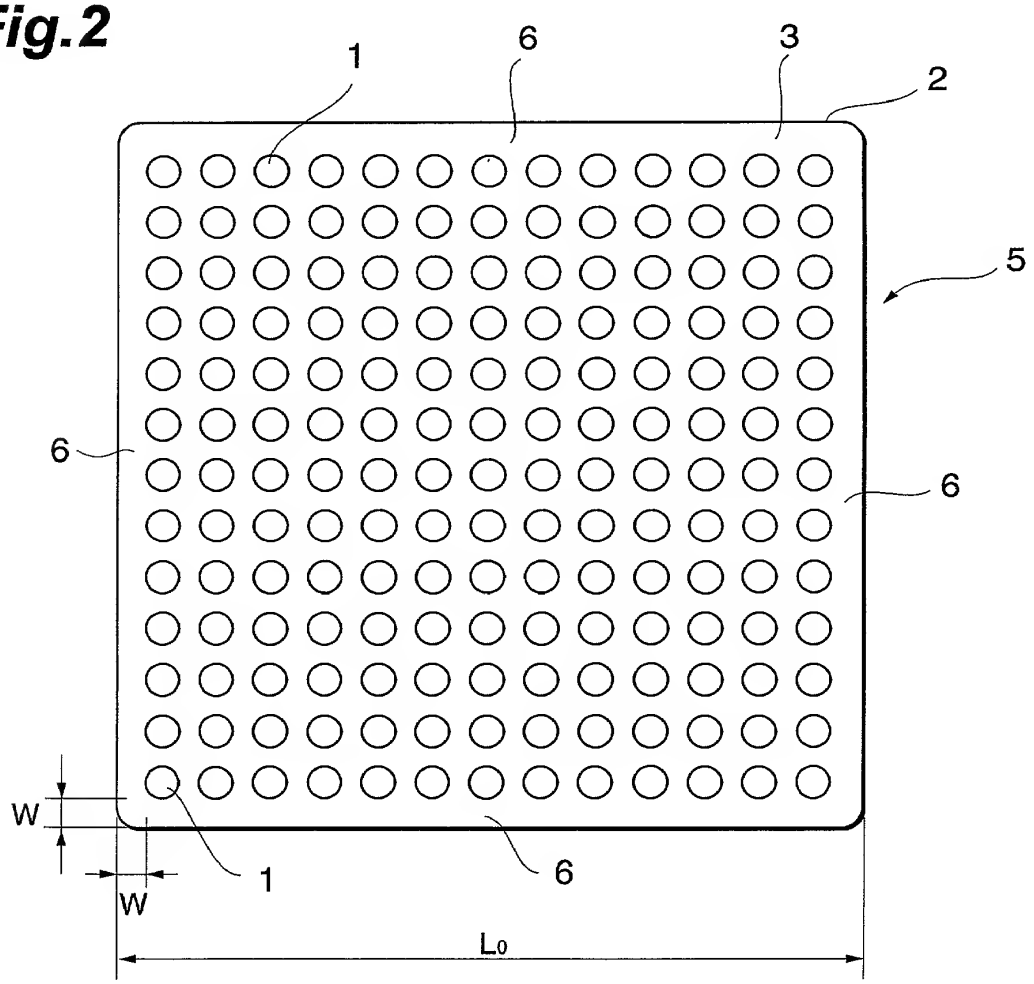


Fig.2



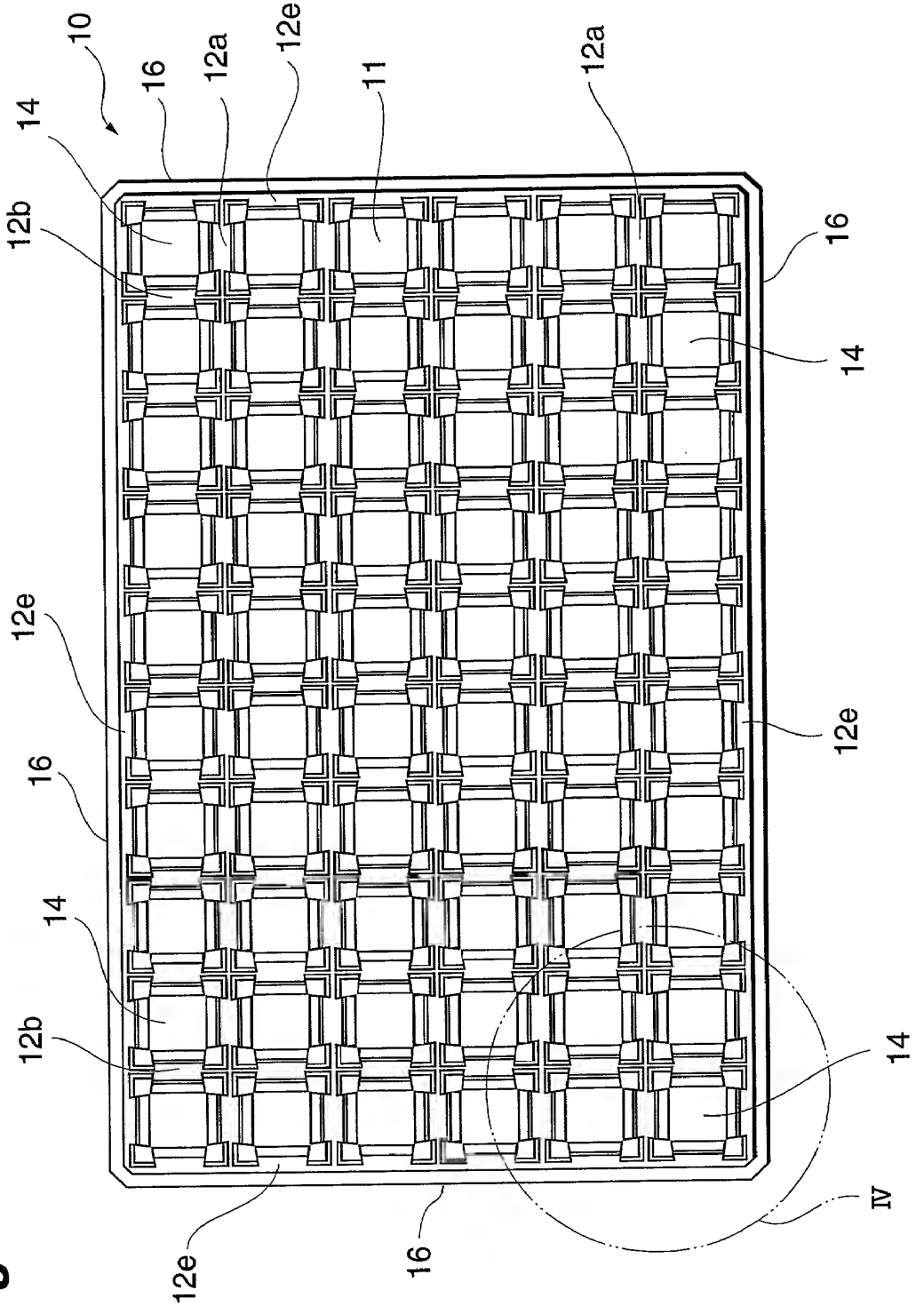


Fig.3

Fig.4

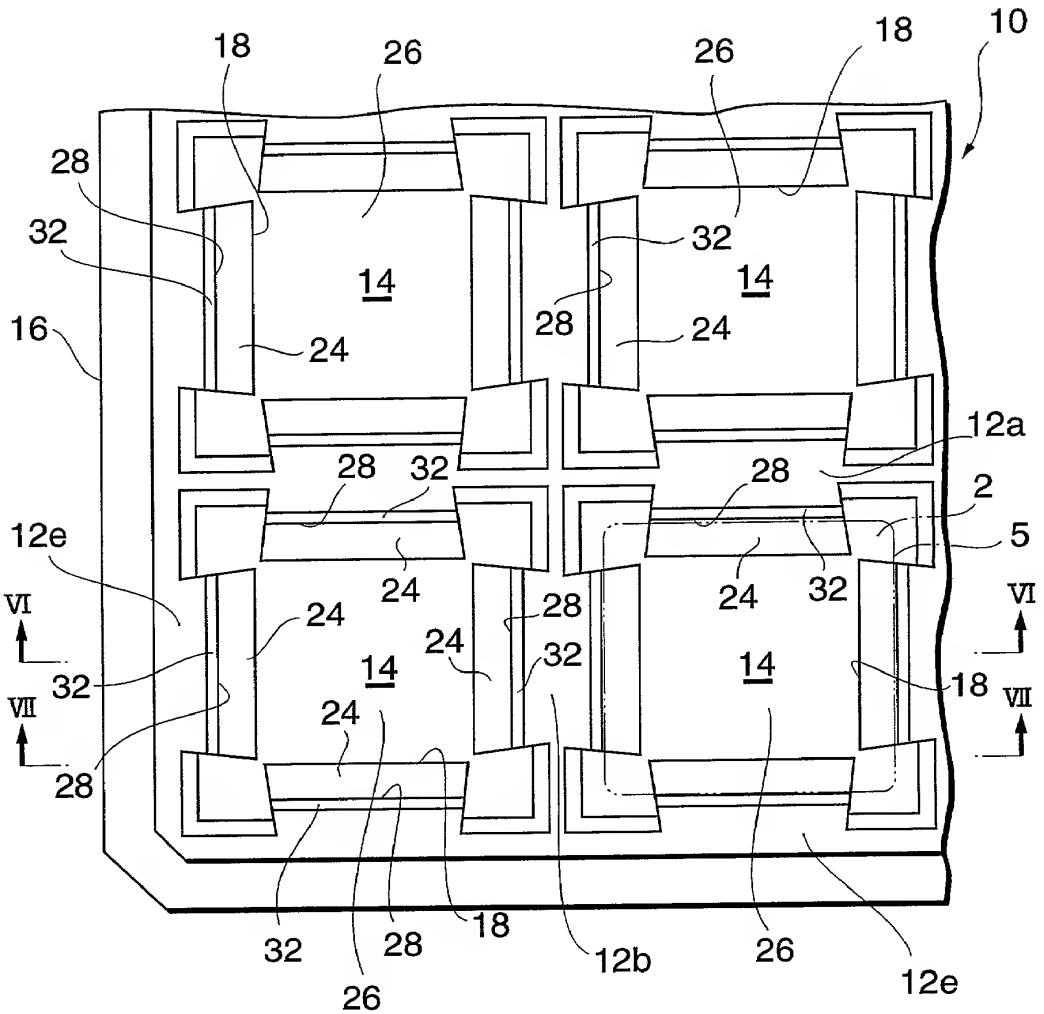

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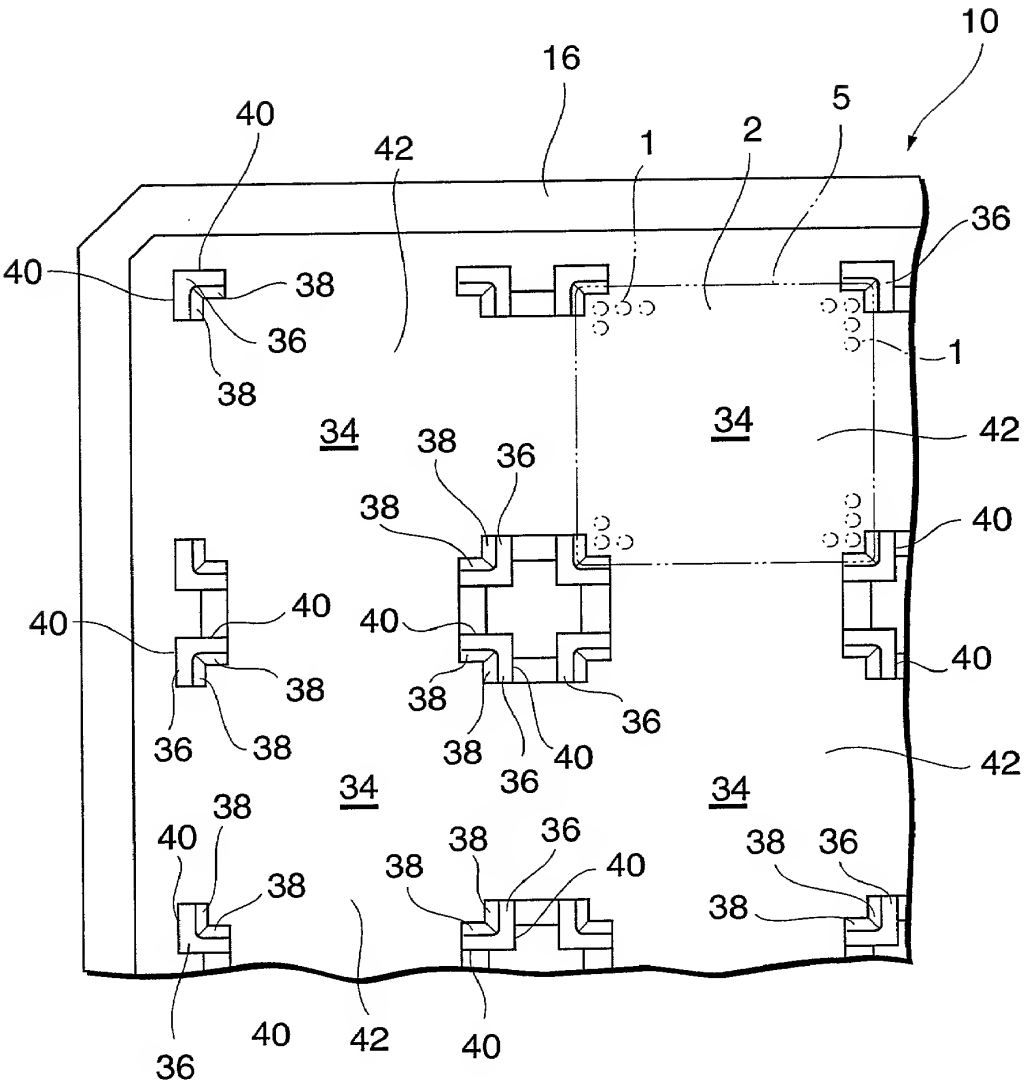
Fig.5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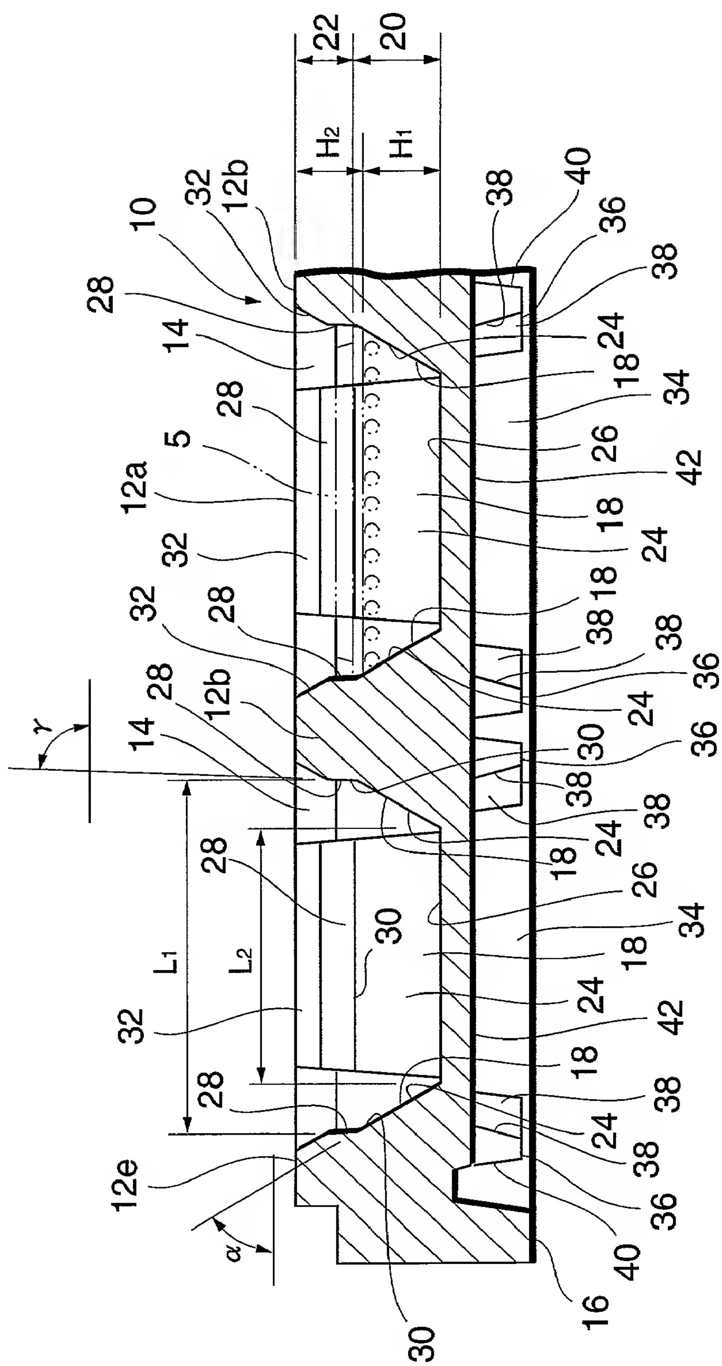

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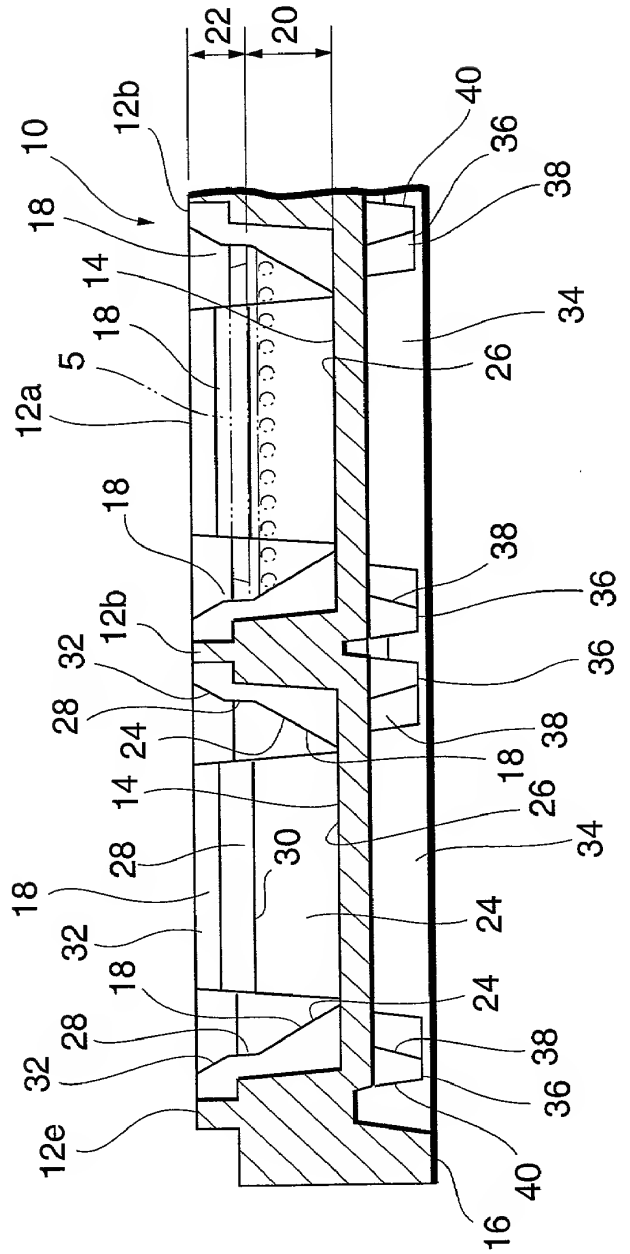
Fig.6

Fig.7



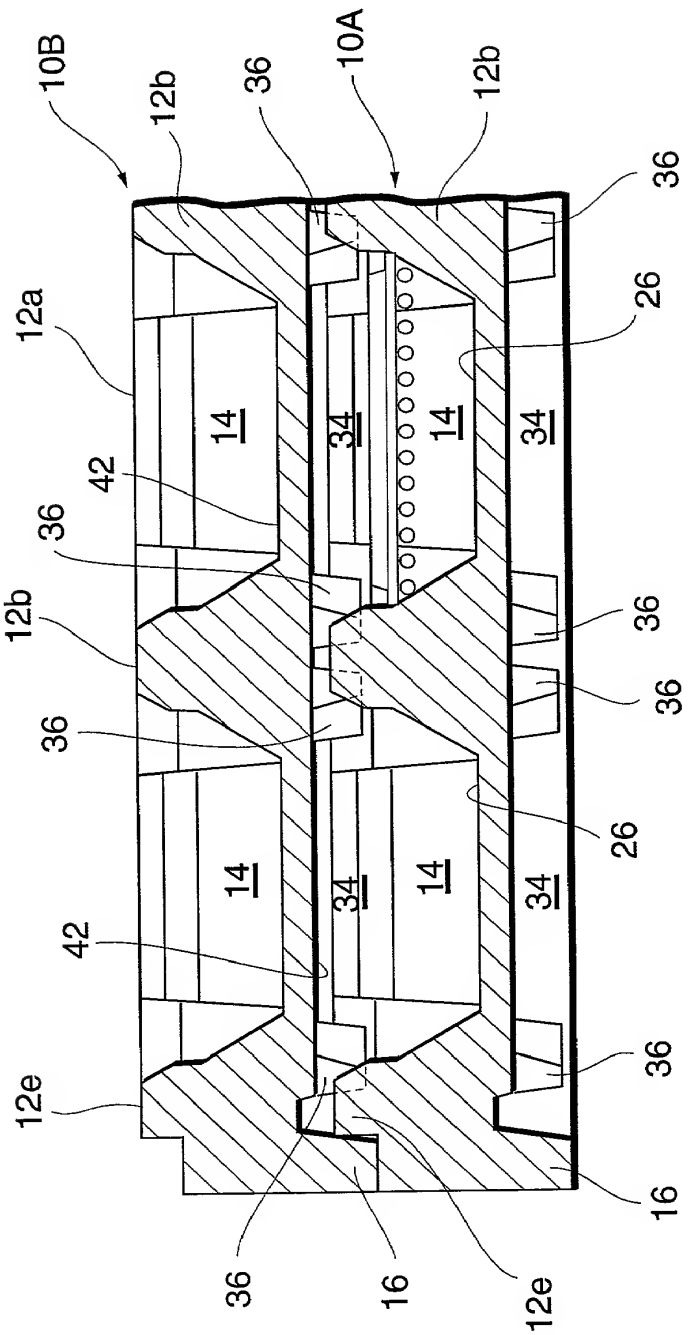


Fig.8

Fig.9

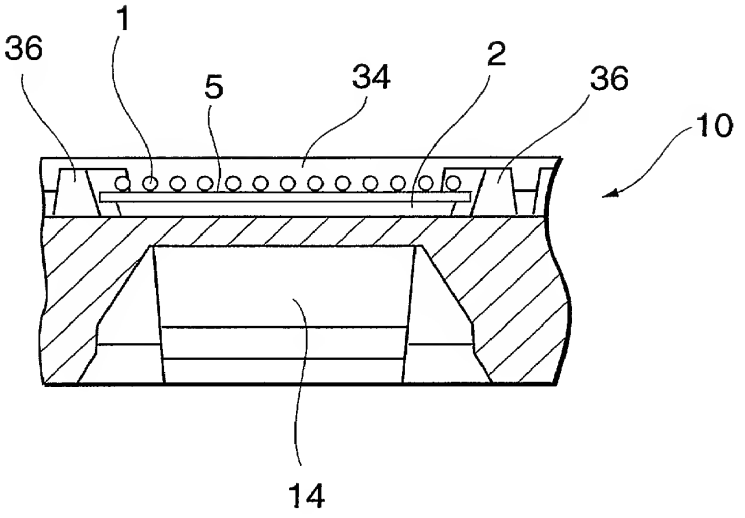


Fig.10

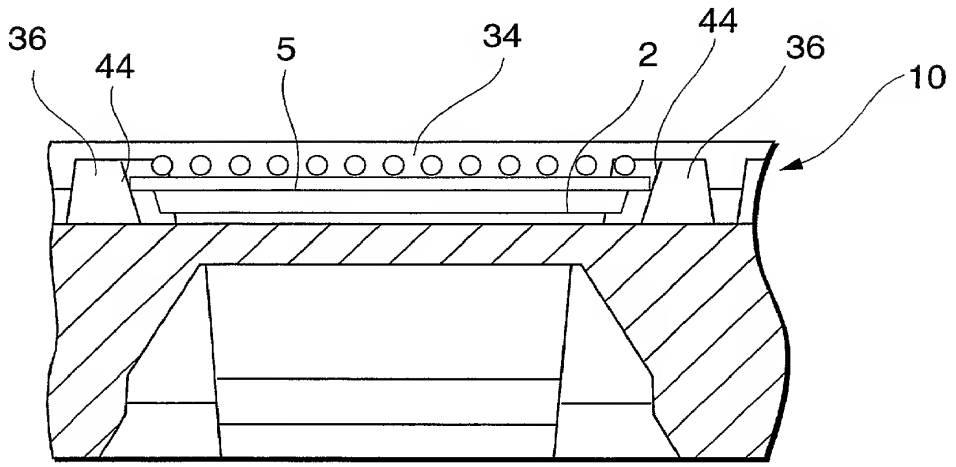
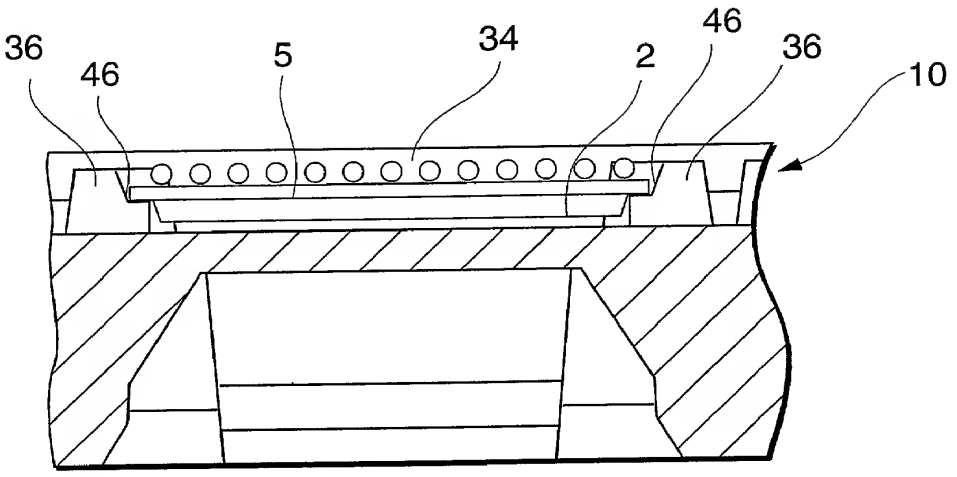


Fig.11



Declaration and Power of Attorney for Patent Application

特許出願宣言書及び委任状

Japanese Language Declaration

日本語宣言書

下記の氏名の発明者として、私は以下の通り宣言します。

As a below named inventor, I hereby declare that:

私の住所、私書箱、国籍は下記の私の氏名の後に記載された通りです。

My residence, post office address and citizenship are as stated next to my name,

下記の名称の発明に関して請求範囲に記載され、特許出願している発明内容について、私が最初かつ唯一の発明者（下記の氏名が一つの場合）もしくは最初かつ共同発明者であると（下記の名称が複数の場合）信じています。

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TRAY FOR SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE

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the specification of which is attached hereto unless the following box is checked:

☐ ___月___日に提出され、米国出願番号または特許協定条約国際出願番号を _____ とし、

☐ was filed on _____ as United States Application Number or PCT International Application Number _____ and was amended on _____ (if applicable).

（該当する場合） _____ に訂正されました。

私は、特許請求範囲を含む上記訂正後の明細書を検討し、内容を理解していることをここに表明します。

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

私は、連邦規則法典第37編第1条56項に定義されるとおり、特許資格の有無について重要な情報を開示する義務があることを認めます。

I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

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私は、米国法典第35編第119条(a)-(d)項又は第365条(b)項に基き下記の、米国以外の国の少なくとも一カ国を指定している特許協力条約第365条(a)項に基づく国際出願、又は外国での特許出願もしくは発明者証の出願についての外国優先権をここに主張するとともに、優先権を主張している本出願の前に出願された特許または発明者証の外国出願を以下に、枠内をマークすることで、示しています。

I hereby claim foreign priority under Title 35, United States Code, Section 119(a)-(d) or 365(b) of any foreign application(s) for patent or inventor's certificate, or 365(a) of any PCT International application which designated at least one country other than the United States, listed below and have also identified below, by checking the box, any freign application for patent or inventor's certificate, or PCT International application having a filing date before that of the application on which priority is claimed.

Prior Foreign Applications
外国での先行出願

(Number) (番号)	(Country) (国名)	Day/Month/Year Filed (出願年月日)	Priority Benefits Claimed? Yes	 No
124326/1999	Japan	April 30, 1999	☒	☐
			☐	☐
			☐	☐
			☐	☐
			☐	☐

私は、第35編米国法典119条(e)項に基づいて下記の米国特許出願規定に記載された権利をここに主張致します。

I hereby claim the benefit under Title 35, United States Code, Section 119(e) of any United States provisional application(s) listed below.

(Application No.) (出願番号)	(Filing Date) (出願日)	(Application No.) (出願番号)	(Filing Date) (出願日)

私は、下記の米国法典第35編第120条に基づいて下記の米国特許出願に記載された権利、又は米国を指定している特許協力条約第365条(c)に基づく権利をここに主張します。又、本出願の各請求範囲の内容が米国法典第35編第112条第1項又は特許協力条約で規定された方法で先行する米国特許出願に開示されていない限り、その先行米国出願書提出日以降で本出願書の日本国内又は特許協力条約国際出願提出日までの期間中に入手された、連邦規則法典第37編第1条第56項で定義された特許資格の有無に関する重要な情報について開示義務があることを認識しています。

I hereby claim the benefit of Title 35, United States Code Section 120 of any United States application(s), or 365(c) of any PCT International application designating the United States, listed below and, insofar as the subject mater of each of the claims of this application is not disclosed in the prior United States or PCT International application in the manner provided by the first paragraph of Title 35, United States Code Section 112, I acknowledge the duty to disclose any material information which is material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56 which became available between the filing date of the prior application and the national or PCT International filing date of this appliation:

(Application No.) (出願番号)	(Filing Date) (出願日)	(Status: Patented, Pending, Abandoned) (現況：特許許可済、係属中、放棄済)

私は、私自身の知識に基づいて本宣言中で私が行う表明が真実であり、かつ私の入手した情報と私の信ずるところに基づく表明が全て真実であると信じていること、さらに故意になされた虚偽の表明及びそれと同等の行為は米国法典第18編第1001条に基づき、罰金または拘禁、もしくはその両方により処罰されること、そしてそのような故意による虚偽の声明を行えば、出願した、又は既に許可された特許の有効性が失われることを認識し、よってここに上記のごとく宣誓を致します。

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Japanese Language Declaration

(日本語宣言書)

委任状：私は、下記の発明者として、本出願に関する一切の手続きを米国特許商標局に対して遂行する弁理士又は代理人として、下記のものを指名致します。(弁護士、又は代理人の氏名及び登録番号を明記のこと)

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith *(list name and registration number)*

John H. Mion, Reg. No. 18,879; Thomas J. Macpeak, Reg. No. 19,292; Robert J. Seas, Jr., Reg. No. 21,092; Darryl Mexic, Reg. No. 23,063; Robert V. Sloan, Reg. No. 22,775; Peter D. Olexy, Reg. No. 24,513; J. Frank Osha, Reg. No. 24,625; Waddell A. Biggart, Reg. No. 24,861; Louis Gubinsky, Reg. No. 24,835; Neil B. Siegel, Reg. No. 25,200; David J. Cushing, Reg. No. 28,703; John R. Inge, Reg. No. 26,916; Joseph J. Ruch, Jr., Reg. No. 26,577; Sheldon I. Landsman, Reg. No. 25,430; Richard C. Turner, Reg. No. 29,710; Howard L. Bernstein, Reg. No. 25,665; Alan J. Kasper, Reg. No. 25,426; Kenneth J. Burchfiel, Reg. No. 31,333; Gordon Kit, Reg. No. 30,764; Susan J. Mack, Reg. No. 30,951; Frank L. Bernstein, Reg. No. 31,484; Mark Boland, Reg. No. 32,197; William H. Mandir, Reg. No. 32,156; Scott M. Daniels, Reg. No. 32,562; Brian W. Hannon, Reg. No. 32,778; Abraham J. Rosner, Reg. No. 33,276; Bruce E. Kramer, Reg. No. 33,725; Paul F. Neils, Reg. No. 33,102; Brett S. Sylvester, Reg. No. 32,765 and Robert M. Masters, Reg. No. 35,603

書類送付先：

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SUGHRUE, MION, ZINN, MACPEAK & SEAS, PLLC
2100 Pennsylvania Avenue, N.W., Washington, D.C. 20037-3202

直通電話連絡先：(名称及び電話番号)

Direct Telephone Calls to: ***(name and telephone number)***

(202)293-7060

唯一又は第一発明者名	Full name of sole or first inventor **Shigeru SEMBONMATSU**
発明者の署名　日付	Inventor's signature　Date April 20, 2000 Shigeru Sembonmatsu
住所	Residence **Tokyo Japan**
国籍	Citizenship **Japan**
郵便の宛先	Post office address **c/o NEC Corporation, 7-1, Shiba 5-chome, Minato-ku, Tokyo 108-8001 Japan**
第二共同発明者名(該当する場合)	Full name of second joint inventor, if any **Manabu ISHIKAWA**
第二発明者の署名　日付	Second inventor's signature　Date
住所	Residence **Ichihara-shi, Chiba Japan**
国籍	Citizenship **Japan**
郵便の宛先	Post office address **Nouman 1389, Ichihara-shi, Chiba 290-0011 Japan**

(第三以降の共同発明者についても同様に記載し、署名をすること。) (Supply similar information and signature for third and subsequent joint inventors.)

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2100 Pennsylvania Avenue, N.W., Washington, D.C. 20037-3202

直通電話連絡先：(名称及び電話番号)

Direct Telephone Calls to: ***(name and telephone number)***

(202)293-7060

唯一又は第一発明者名	Full name of sole or first inventor **Shigeru SEMBONMATSU**
発明者の署名　日付	Inventor's signature　Date
住所	Residence **Tokyo Japan**
国籍	Citizenship **Japan**
郵便の宛先	Post office address **c/o NEC Corporation, 7-1, Shiba 5-chome, Minato-ku, Tokyo 108-8001 Japan**
第二共同発明者名(該当する場合)	Full name of second joint inventor, if any **Manabu ISHIKAWA**
第二発明者の署名　日付	Second inventor's signature　Date Manabu Ishikawa　Apr. 19, 2000
住所	Residence **Ichihara-shi, Chiba Japan**
国籍	Citizenship **Japan**
郵便の宛先	Post office address **Nouman 1389, Ichihara-shi, Chiba 290-0011 Japan**

(第三以降の共同発明者についても同様に記載し、署名をすること。) (Supply similar information and signature for third and subsequent joint inventors.)